Innovations in Fan Out Packaging for Mobile Applications

John Hunt
ASE Group
April 16, 2015
Global Connectivity Acceleration

<table>
<thead>
<tr>
<th></th>
<th>2003</th>
<th>2012</th>
<th>2015</th>
<th>2020</th>
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<tbody>
<tr>
<td>World Population</td>
<td>6.3 Billion</td>
<td>7.0 Billion</td>
<td>7.2 Billion</td>
<td>7.6 Billion</td>
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<tr>
<td>Connected Devices</td>
<td>500 Million</td>
<td>8.7 Billion</td>
<td>18.2 Billion</td>
<td>50 Billion</td>
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<tr>
<td>Connected Devices per Person</td>
<td>0.08</td>
<td>1.24</td>
<td>2.53</td>
<td>6.58</td>
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</table>

Source: Cisco 2013
iPhone Trends: Increasing Number of WLPs

<table>
<thead>
<tr>
<th>iPhone Model/year</th>
<th>WLPs</th>
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<tbody>
<tr>
<td>iPhone 1 2007</td>
<td>2</td>
</tr>
<tr>
<td>iPhone 3GS 2009</td>
<td>4</td>
</tr>
<tr>
<td>iPhone 4S 2011</td>
<td>7</td>
</tr>
<tr>
<td>iPhone 5 2013</td>
<td>11+</td>
</tr>
<tr>
<td>iPhone 5S 2013</td>
<td>22</td>
</tr>
<tr>
<td>iPhone 6 2014</td>
<td>26+</td>
</tr>
<tr>
<td>iPhone 6 Plus 2014</td>
<td>26+</td>
</tr>
</tbody>
</table>

Shown to scale

Source: TechSearch International, Inc., adapted from TPSS.
Drivers for Advanced Packaging

Drivers

- Small, Thin for mobile applications
- Low cost for Consumer Products
- Good Electrical performance
- Low power

Solutions

- Wafer Level Chip Scale Package
- Fanout Wafer Level Package
- Fanout Chip Last Package
Drivers for Fan out

- **Die Shrinkage**
  - Advanced Technology nodes allow die shrinkage
    - Increased die per wafer & lower individual die price
    - But - Less die area for Ball placement
  - Fan out allows expansion of ball placement area beyond die borders
    - Fan out cost offset by lower die pricing
    - Retain Ball footprint of larger die WLCSP

- **Multi-Die & Inclusion of Passives**
  - Advanced Technology nodes increases wafer cost for high technology nodes
    - Not all die functionality benefits from advanced nodes
      - Power
      - Analog
  - Fan out allows Partitioning of functionality within a package
    - Digital functions can use advanced technology nodes
    - Analog, Power, MEMS, IPDs can use lower technology nodes
    - Fan out allows these various nodes to be embedded in same package
    - Passives can also be embedded in Fan out package to form SIPS
Fan out Technology
Fanout Embedded Packaging

- Embedding moves the die from the surface of a package, and “embeds” it inside a polymer or other material matrix.
ASE Fan out Strategy

Panel Fan out
(In Development)
Fan Out Chip Last

Embedded Package
Wafer Level Fan out
Package on Package
Fan Out Chip Last

High Density
Wafer Level Fan out
2.1/2.5/3D Package
Wafer Chip Last

Low
Middle
High

chip First – Embedded Chips

Cost Driven
Median Level
Performance Driven

Driver
Technology
Chip Last – Flip Chip
Fan out Wafer Level Package
aWLP
aWLP Fan out Wafer Level Package

Traditional Fan-In WLCSP

Fan-Out WLP (FOWLP)

Die are embedded in a “Reconstituted” plastic wafer that is processed like a Silicon wafer
aWLP Basic Process Flow

Wafer Saw

Wafer Redistribution

Wafer Reconstitution

aWLP Package with Solder Balls & Singulated
aWLP Wafer Reconstitution Process Flow

1. Lamination of tape onto carrier
2. Die Placement
3. Wafer Molding
4. Wafer Debonding
5. Tape removal

Heating stages are indicated by red arrows.
aWLP Reconstituted Wafer
Evolutionary Paths for Wafer Level aWLP

- Single Die aWLP (HVM)
- Multi Die 2D aWLP (Qualified)
- Multi Die 2D with Passives aWLP (Prototype)
- Double sided 3D aWLP Module Assembly (Prototype)
- Double sided 3D aWLP Package on Package (Prototype)
3D Fanout Development

- Embedded 3D TSV Via Die gives higher density and improved multilayer routability without multiple RDL Layers
- Can include cross routing and Integrated Passives into interposer
3D aWLP Stacked POP

3D aWLP Bottom
490μm

3D aWLP Top

3D aWLP Stacked POP
aWLP 3D Double Sided Development

- 3D aWLP Package with Embedded TSV Die - 500µm Thick
Advanced aWLP (Fan Out Chip on Substrate - FOCoS)

- Structure is an Advanced Flip Chip BGA package using Fan out
- Market Drivers
  - Integration of multiple chips: Either with same advanced wafer nodes or with different wafer nodes
  - Faster time to market
- Package Selection
  - Alternative to 2.5D Silicon Interposer technology
- Initial Application
  - MultiDie in aWLP on FC Substrate
  - 16nm & 28nm Die
  - > 40 x 40mm Package with SnAg Bumps
  - I/O > 1000
  - Lines/Spaces <3/3µm
  - 3 RDL layers
Advanced FOCoS

Stacked Vias:

Fine RDL Lines/Spaces:
Advanced FOCoS

- 2-Die FOCoS
Panel Level Fanout
Embedded Package
ASE Fanout Panel Development

- Panel Fanout
  - ASE is developing a panel process version of fanout packaging
  - Focusing on lower pin count, Higher Power fanout packages
  - Initial prototypes passed all package & Board level reliability

30µm Laser Via
Process Flow - Panel Fanout

1. Wafer Preparation
2. Cu UBM Formation
3. Carrier Alignment Key Prep
4. Adhesive/Die Placement
5. Dielectric Lamination
6. Laser Via Formation
7. Plating Vias/RDL
8. Solder Resist
9. Ball Mount & Saw
Single Die Prototype

Single Die Fanout Panel Level Package

<table>
<thead>
<tr>
<th>Schematic</th>
<th>Item</th>
<th>X-section of Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Solder Resist</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>RDL</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Interconnection (blind via)</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Encapsulation</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Chip I/O</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Chip</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Adhesive</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Carrier</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Maximum Package height (without solder ball): 430 um

Package Specification:

- Package size: 8 x 8 mm
- Die size: 3.1 x 3.1 mm
- Package THK: 430 um
- Die THK: 150 um
- Die I/O: 196
- Die pad pitch: 200 um
- Ball pitch: 400 um
- L/S: 20/20 um
- Blind via diameter: 70um
2D 2-die Panel Fanout Package

Package Specification

- Package size: 8x8 mm
- Die size: 3.1x3.1 mm x 2
- Package THK: 400 µm
- Die THK: 150 µm
- Die I/O: 196
- Die pad pitch: 200 µm
- Ball pitch: 400 µm
- L/S: 20/20 µm
- Blind via diameter: 70µm

Top view of RDL pattern: L/S 20/20µm

Interconnection of RDL to Chip thru blind via

X-section of 2D Package
Double-sided Panel Fanout Package

- Technology extension for 3D or multi-die packages
- Package-on-Package (PoP)
- Multi-chip module (MCM)

Process Flow:

1. Core layer
2. Mechanical drill
3. Pattern formation
4. Cu stud formation
5. Adhesive dispensing & die placement
6. Dielectric lamination
7. Blind via formation
8. Pattern formation
9. Solder Resist
10. Ball mount & Saw
Package Level Reliability

- The single die package passed all JEDEC Package Level Reliability tests

<table>
<thead>
<tr>
<th>Package Specification</th>
<th>Lot1</th>
<th>Lot2</th>
<th>Lot3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package size: 8 x 8 mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Die size: 3.1 x 3.1 mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package THK: 430 um</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Die THK: 150 um</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Die I/O: 196</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Die pad pitch: 200 um</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ball pitch: 400 um</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L/S: 20/20 um</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Blind via diameter: 70um</td>
<td></td>
<td></td>
<td></td>
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</table>

<table>
<thead>
<tr>
<th>Reliability condition</th>
<th>Lot1</th>
<th>Lot2</th>
<th>Lot3</th>
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</thead>
<tbody>
<tr>
<td>Pre-condition</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T/C cycle: -55°C - 125°C, 5x</td>
<td>Passed</td>
<td>Passed</td>
<td>Passed</td>
</tr>
<tr>
<td>Baking: 125°C, 24hrs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MSL3: 30°C, 60% RH, 192 hrs</td>
<td>Passed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reflow: 260°C, 3x</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HAST</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- 130°C/85%RH, 33.5 psig, 96/192 hrs</td>
<td>Passed</td>
<td>Passed</td>
<td>Passed</td>
</tr>
<tr>
<td>TCT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- -55°C ~ 125°C</td>
<td>500/1000x</td>
<td>Passed</td>
<td>Passed</td>
</tr>
<tr>
<td>HTST</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- 150°C, 500/1000 hrs</td>
<td>1500x</td>
<td>Passed</td>
<td>Passed</td>
</tr>
<tr>
<td></td>
<td>Passed</td>
<td>Passed</td>
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</tbody>
</table>
The single die package passed all JEDEC Board Level Reliability tests, including 2000 TCOB cycles.

- **Package Specification**
  - Package size: 8 x 8 mm
  - Die size: 3.1 x 3.1 mm
  - Package THK: 430 um
  - Die THK: 150 um
  - Die I/O: 196

  - Die pad pitch: 200 um
  - Ball pitch: 400 um
  - L/S: 20/20 um
  - Blind via diameter: 70 um

<table>
<thead>
<tr>
<th>Reliability item</th>
<th>Condition</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drop Test</td>
<td>30 times (JESD22-B111)</td>
<td>Passed</td>
</tr>
<tr>
<td>Thermal cycle</td>
<td>-40°C ~ 125°C, 500/1000/1500/2000x (JESD22-A104C)</td>
<td>Passed</td>
</tr>
</tbody>
</table>
How do we take the cost out of 
**Fan Out Packaging?**

And make it 
**Highly Manufacturable?**
Fan out Chip Last Coreless Package
Fan Out Chip Last Package

- Low Cost Coreless Substrate
- Cu Pillar Bumps
- Embedded Traces
- Flip Chip Mass Reflow
- Mold Only Underfill

Low Cost Fan Out Package!
Chip First FOWLP vs Chip Last FOCLP

- **Chip First FOWLP**
  - Process/Structure where die are first embedded in mold compound in the form of a standard Silicon wafer, with Redistribution circuitry formed after molding onto the surface of the mold compound, expanding the area available for Solder Balls or LGA pads.

- **Chip Last FOCLP**
  - Process/Structure where die are first Copper Pillar bumped, and then Flip Chipped using Mass Reflow and MUF onto a pre-existing Redistribution circuitry formed as a coreless substrate with embedded traces, expanding the area available for Solder Balls or LGA pads.
Paradigm Shift: Fan out Chip Last Package

- Utilizing **Low Cost FC Coreless Substrate**
  - Embedded Traces & Pads
  - Fine Pitch capable

- Combined with Mass Reflow fine pitch Cu Pillar FC & Molded Underfill (MUF)

- Creates new Paradigm in low cost Fan out Packaging
  - Low Cost Coreless Substrate
  - Chip Last vs Chip First for Higher Assembly yields
  - Fine Pitch bumping direct on die pad without RDL
  - Thicker Copper (15-50µm) allows higher current
  - Thin Package < 375µm
  - MSL 1
• Cost effective Fan Out Chip Last Package
• Known Good Die assembly on Known Good Substrate - new embedded trace FOCLP:
Panel Size: 510x410 mm (209,100mm²) X 2
Strip Size: 240x76.2 mm (X2L)
Strip Array: 34x13 => 442 ea

Wafer size: 300mm(70,686mm²)

6X Area

No FO Wafer Fab investment needed, ASE uses standard FlipChip Packaging
Different Process – Same End Product

FOCLP can be identical in size, thickness, foot print, trace layout and performance as FOWLP
FOCLP Attributes (Rev)

Typical FOCLP Dimensions
(Not to Scale)

Drawn to Scale

FOWLP Slim 2
FOWLP Slim 2-T2
FOCLP

<table>
<thead>
<tr>
<th>FOCLP</th>
<th>Bump Pad Pitch</th>
<th>Lines Passing Thru</th>
<th>L/S</th>
<th>Die to Pkg Edge</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Production</td>
<td>80µm</td>
<td>100µm</td>
<td>125µm</td>
<td>16x16µm</td>
</tr>
<tr>
<td>Advanced</td>
<td>60µm</td>
<td>80µm</td>
<td>110µm</td>
<td>15x15µm</td>
</tr>
<tr>
<td>Engineering</td>
<td>50µm</td>
<td>70µm</td>
<td>90µm</td>
<td>12x12µm</td>
</tr>
</tbody>
</table>
Multi Die/Passive SIP FOCLP

- Multiple actives and passives can easily be included in FOCLPs using existing volume production equipment
Fan Out Chip Last Example

- FO Package originally designed for FOWLP process/structure
- Design transferred directly into FOCLP process/structure
- Multi-Die Fanout Package
FOCLP Example - Results

- **Package Level Reliability**
  - Passed MSL 1
  - Passed TCT 1000 cycles, PCT 168 Hrs, HAST 168 Hrs

- **Board Level Reliability**
  - Drop Test – Passed 150 Drops (test ongoing)
  - Temperature Cycling – ongoing

- **Biased HAST results**
  - Passed
  - No Change in Resistance values
  - All Bias Voltages passed

- **Warpage**

<table>
<thead>
<tr>
<th></th>
<th>TCT 500 cycles</th>
<th>TCT 1000 cycles</th>
<th>PCT 96 hr</th>
<th>PCT 168 hr</th>
<th>HAST 96 hr</th>
<th>HAST 168 hr</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>SAT</td>
<td>SAT</td>
<td>SAT</td>
<td>SAT</td>
<td>SAT</td>
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<tr>
<td>MSL 1</td>
<td>66/66 pass</td>
<td>66/66 pass</td>
<td>22/22 pass</td>
<td>22/22 pass</td>
<td>22/22 pass</td>
<td>22/22 pass</td>
</tr>
<tr>
<td>MSL 2</td>
<td>66/66 pass</td>
<td>66/66 pass</td>
<td>22/22 pass</td>
<td>22/22 pass</td>
<td>22/22 pass</td>
<td>22/22 pass</td>
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<tr>
<td>MSL 3</td>
<td>66/66 pass</td>
<td>66/66 pass</td>
<td>22/22 pass</td>
<td>22/22 pass</td>
<td>22/22 pass</td>
<td>22/22 pass</td>
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<tr>
<th>S.S.</th>
<th>0hr 96hrs</th>
<th>0hr 96hrs</th>
<th>0hr 96hrs</th>
<th>0hr 96hrs</th>
<th>0hr 96hrs</th>
<th>0hr 96hrs</th>
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<tbody>
<tr>
<td>1</td>
<td>106.3</td>
<td>106.3</td>
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<tr>
<td>3</td>
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<td>106.3</td>
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</tbody>
</table>
Production FOCLP Variations

All are variations of Volume Production Products using FCCSP technology today
The Manufacturing Infrastructure is already in Place
FOCLP for Wirebond

- Fan Out Chip Last can be used with Cu Pillar or Wirebond die
- WB die uses NiAu on coreless substrate pads
Also WLCSP - Fan In Chip Last Package (FICLP)

- WLCSP - Chip Last with coreless substrate can also be used for Fan In applications
- Can be more cost effective for larger die than WLCSP
- Attributes
  - FICLP ~200µm larger in X & Y than bare die
  - Molded package <=165µm or less in thickness
  - 50µm die pad pitch
  - Better reliability than large WLCSP
    - Cu Pillar with underfill isolates solderballs from die
    - Mold Compound surrounds die on all 6 sides
  - Higher current carrying capacity than WLCSP
Advantages of Fan out Chip Last

- In High Volume Production
- Uses existing FCCSP infrastructure
  - No investment in Wafer level equipment for processing
- Low Cost coreless Substrate
  - Manufactured in double panel format, Assembled in strip form
- Can be used for Fan Out or Fan In applications in Low to Medium Complexity FO Packages
- All variations of high volume production with standard Flip Chip Processes
  - Multi-Die
  - Passives
  - Double-sided/POP
- Can be thinner than FOWLP
- Higher current & thermal handling capabilities – thicker Copper available
- Better reliability performance
  - Underfill/isolation of solderballs from Die surface
Multiple ASE Paths for Fan out

Fan Out Wafer Level Package

Fan Out Chip Last Package
ASE is evolving new packaging innovations for miniaturization, performance, and cost improvements.

- WLCSP (Wafer Level Chip Scale Package)
- Fan Out Wafer Level Package
- Fan Out Chip Last Package

System Integration into SiP (System in Package)
Thank You

www.aseglobal.com