Challenges & Opportunities for 3DIC TSV Based Products

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Stacked CSP – Migration to TSV

Stacked CSP

FlipStack® CSP

F2F FlipStack®

TSV Stacked CSP
FCBGA – Migration to TSV

Logic with Embedded Memory

Logic and Memory in Same Module

Logic and Memory in Separate Packages

TSV Stacked BGA
TSV Industry Product Development

- **Vertical Stacking**
  - Many top tier customers engaged with several years of development completed
  - Today CSP focused on 28nm CMOS… scaling to 20/22nm
  - Both wafer finishing and pre-finished wafer process flows being used

- **Interposer – Side by Side Stacking**
  - Many top tier customers engaged with several years of development completed
  - All large package body focused
  - Both wafer finishing and pre-finished wafer process flows being used
  - Logic on Interposer
    - Multiple logic die on single thinned interposer
  - Logic + Memory on Interposer
    - Single logic die + multiple memory stacks on single thinned interposer
    - Other passive components in some cases
Die with SV indicated by = T

All Products planning on 22/20nm in future platforms for TSV
3DIC TSV Product Opportunities

- Focus process node development on specific application functionalities
- Reduces complexity and mask layer count of process node
- Reduces advanced process node ‘Time to Market’
- Improves wafer yield
- Reduces wafer start cost
- Improves performance, power, and area of each application functionality
### Primary Drivers for Interposers

<table>
<thead>
<tr>
<th>Si Interp(^T) + DDR(^T) + Logic</th>
<th>Memory Bus Speed</th>
<th>Lower Power</th>
<th>Fab Yield</th>
<th>New Markets</th>
<th>Stress Reduction in Top Die</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Wide Parallel Busses</td>
<td>Wide Parallel Busses</td>
<td>Departition</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td><strong>Si Interp(^T) + Logic</strong></td>
<td><strong>Gate to Gate Routing between Die</strong></td>
<td><strong>Deconstruc	 Smaller Die</strong></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td><strong>Si Interp(^T) + Logic + SERDES</strong></td>
<td><strong>Departition (e-DRAM)</strong></td>
<td><strong>Integrate Heterogeneous Die</strong></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>
**Silicon Interposer Logistic Challenge**

**Business Concerns:**
- Ownership of TSV related failures
- Cost
- Agreed to metric for known good Wafer

**Technical Concerns:**
- BOM Compatibility
  - Same bump metallurgies
  - Same passivation materials
- Thin wafer handling / shipping

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**Diagram:**
- **Foundry/IDM** → **Vias Early** → **Front Side NiPdAu Pad** → **Wafer Finish**
  - Can be at either Foundry or OSAT
  - **Send to SAT** → **SAT** → **Wfr Support** → **Thin** → **Back Side Bump** → **Debond** → **Ship**

- **Continue at Foundry** → **Wfr Support** → **Thin** → **Back Side Bump** → **Debond** → **Ship**
TSV Product Challenges
Technology Integration

- Thermal
- Micro Copper Pillar Bumping
- Micro Joining
- Silico Interposer
- Underfill
- Interposer Thinning
- Thin Wafer Handling
- Subassembly & Package Warpage
Wafer Finishing of TSV Devices

- **TSV Reveal, Isolation and Passivation**
  - Key: No damage to silicon, liner or tip
  - Critical: No copper residue on surface

**Grind – Expose TSV**

**Silicon Etch Recess**

**Ni – Au on Copper Via**
Wafer Finishing of TSV Devices, cont.

Back Side Pad Metal

Liner Intact /un-Damaged

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Amkor Info. for Controlled Release at AZ IMAPS 11  R.Huemoeller Oct-11
Top Wafer Finishing Challenge
Thin Wafer Handling

- **200/300mm Thin Wafer Handling – De-bonding**
  - De-bonding both 200mm and 300mm wafers with large C4 bumps on back side of wafer very challenging
  - Wafer breakage, bump deformation, foreign material all present challenges
Top TSV Assembly Challenges

- **Die-Die / Die-Substrate Joining**
  - Micro bump uniformity; Method of Join; Materials

- **Die-Die X-Y Spacing**
  - Fillet sizes and pad metallurgy
  - Process assy sequence; Micro-join method & Mat’ls

- **Thermal & Power Management**
  - Use of Lids, Stiffeners & Passives
  - Underfill/Resin bleed, adhesive compatibility
  - Process assy sequence; Micro-join method & Mat’ls

- **Warpage Control**
  - Interposer warpage; Substrate warpage
  - Top die warpage – top die area density/distribution

- **Intermediate e-Test Points**
  - Process assembly sequence

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Assembly Process Flexibility is REQUIRED

Die to Die
Die to Substrate
Die to Wafer
Many Assembly Flows in Use Today

Small Die Flows

#1 M.Reflow + CUF
#2 TC Bond + NCP

Vertical Stacking

#1 D2D M.Reflow
#2 D2S M.Reflow

#3 D2S TC/NCP & M.Reflow
#4 D2S ALL TC/NCP
#5 D2S M.R & TC/NCP

Large Die Flows

Side-Side Stacking

Die Attach to Substr
Reflow
Capillary Underfill
Next Die TC + NCP
Final Test

TC + NCP Die - Subst
Reflow
Capillary Underfill
Next Die TC + NCP
Final Test

Die Attach to Interp
Reflow
Capillary Underfill
Attach Die Stack to Sub
Reflow
Capillary Underfill
Final Test

Interp to Sub Attach
Reflow
Capillary Underfill
Die attach to interp
Reflow
Capillary Underfill
Final Test

TC + NCP Interp to Sub
Reflow
Capillary Underfill
Die attach to interp
Reflow
Capillary Underfill
Final Test

TC + NCP Interp to Sub
Reflow
Capillary Underfill
TC + NCP Next Die(s)
Reflow
Capillary Underfill
Final Test

Interp to Sub Attach
Reflow
Capillary Underfill
TC + NCP Next Die(s)
Reflow
Capillary Underfill
Final Test
TSV CSP Vertical Assembly

- **Thermo-Compression Bond + Non Conductive Paste (NCP)**
  - Thin die handling capability to 50µm
  - Material dispense critical

Pitch $\geq 40\mu m$ today; 30µm 2011
Pillar to Ni-Au Pad as standard

Cu Pillar with SnAg µBumps
40µm today
T SV Silicon Interposer Assembly

- **Assembly Experience on Interposer**
  - Substrates range from 35mm up to 55mm
  - Interposer thickness as thin as 60um, but typically at 100um

Pitch ≥ 40µm today; 30µm 2012

80µm Tall Plated SnAg Bumps
Pitch ≥ 150µm today; ≥ 130µm 2012
TSV Silicon Interposer Reliability

- Initial Underfill
- MRT, L4
- HAST 48 Hours
- HAST 264 Hours

Passed MRT + HAST: 110C, 85% RH, 264 Hours

Courtesy of Xilinx, TSMC, Amkor
TSV Reliability Data – General

• **ASIC (die to die = face to face)**
  – Multiple Die on Interposer ; 100µm thick, 10µm TSV at 210µm pitch
  – Logic at 40µm pitch µbump with 25µm dia. ; over 200k micro-bumps
  – Passed Level 4 MRT ; TC Condition B 1000 cycles ; HTS 1000 hrs

• **Handset – 45nm Baseband (die to die = face to back)**
  – Memory ~ 100µm thick
  – Logic ~ 50µm thick with 10µm TSV at 40µm pitch ; either peripheral or area array bump pitch to substrate
  – Passed MRT L3 260°C (3x reflow) ; T/C-B 1000 cycles ; HTS 1000 hrs
Thank You!