Enabling a New Class: The Panel Level SoC

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Tim Olson - Founder & CTO

Deca Technologies
Changing Form

X-ray images courtesy of Nick Veasey & flickr.com
Smartphone Sales Have Overtaken PCs

The Graph shows the changing form of smartphone and desktop & notebook PC shipments from 2008 to 2017. The y-axis represents shipments in millions, and the x-axis represents the years from 2008 to 2017.

- **Smartphones** have shown a significant increase in shipments, overtaking PCs by 2012.
- **Desktop & Notebook PCs** have maintained a steady but declining trend in shipments.

The Post-PC Era

Sources: Gartner, Statista & IDC
Electronic Interconnect
Different industries serving different levels

FOUNDRY

SATS

EMS

Device
(Chip Level)

Package
(1st Level)

System
(2nd Level)

SATS & EMS images courtesy of Prismark & Chipworks

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Enabling a New Class: The Panel Level SoC
Electronic Interconnect
Chip Level – The SoC (System on a Chip)
Electronic Interconnect
Chip Level – The SoC

**IP Blocks**
- MCU core(s)
- Power Mgmt
- Flash
- SRAM
- ADC, DAC
- NVM

**Interfaces**
- DRAM
- SRAM
- I²C
- SPI

**RF Functions**
- Tx, Rx
- BB

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Enabling a New Class: The Panel Level SoC
Electronic Interconnect ...
Different industries, different dimensions

- **Device**
  - Nanometers

- **Package**
  - Microns

- **System**
  - Millimeters

Decca Technologies
Enabling a New Class: The Panel Level SoC
... coming from different financial backgrounds

**Capital Intensity**
(Annual capex ÷ Annual revenue)

**Gross Margin%**

**Operating Income%**

Source: SEC filings from company websites
... yet historical supply chain boundaries are blurring
Enabling a New Class: The Panel Level SoC

... while costs remain quite different

<table>
<thead>
<tr>
<th>Chip Level Electronic Interconnect</th>
<th>Typical Geometries</th>
<th>Typical Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital processor</td>
<td>20 nm</td>
<td>6 ¢ per mm²</td>
</tr>
<tr>
<td>Analog</td>
<td>55 to 130nm</td>
<td>3 ¢ per mm²</td>
</tr>
<tr>
<td>RF</td>
<td>65 to 180nm</td>
<td>2 ¢ per mm²</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>1st Level Electronic Interconnect</th>
<th>Typical Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flip chip CSP packaging</td>
<td>0.7 ¢ per mm²</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>2nd Level Electronic Interconnect</th>
<th>Typical Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 layer Smartphone motherboard</td>
<td>0.4 ¢ per mm²</td>
</tr>
</tbody>
</table>
What if ... the functional blocks of an SoC

... were disintegrated
... and re-integrated in a new way
... and re-integrated in a new way
... utilizing fan-out technology to connect functional blocks

... routing across mold compound to create a panel level SoC

Deca Technologies
Panel Level SoC: a group of disparate semiconductor functional blocks embedded within mold compound enabling panel level electronic interconnect to create a virtual SoC
Transforming Electronic Interconnect

Enabling a New Class: The Panel Level SoC

... defining the panel level SoC

**Panel Level SoC**

: a group of disparate semiconductor functional blocks embedded within mold compound enabling panel level electronic interconnect to create a virtual SoC
... it all comes down to cost, can panel based fan-out deliver?

Technology Cost Comparison
(Sales price to customers)

- Adv Si: 6 cents per mm²
- Analog Si: 3 cents per mm²
- RF Si: 2 cents per mm²
- FC CSP: 0.7 cents per mm²
- OEM PCB: 0.4 cents per mm²

Panel Fan-out Potential
... scaling the manufacturing format is key to cost

Initial production

300mm round

Future Production*

Large panel format

*Note: Patents issued & pending
Transforming Electronic Interconnect

Enabling a New Class: The Panel Level SoC

... overcoming the barriers, capital cost & yield

- **Wafer fab cost breakthrough**
  
  *Wafers fabricated on non-fab capital equipment*

  **Inspired by**

  ![SunPower Logo](image)
  
  *SUNPOWER*
  
  Solar wafer fab manufacturing

- **Yield & chip attach cost breakthrough**
  
  *Die placement at high speed with a low cost of capital & high yield*

  **Enabled by**

  ![Adaptive Patterning Logo](image)
  
  *Adaptive Patterning*

  ![Deca 4x4mm² Package Image](image)

  **Deca 4x4mm² Package**

<table>
<thead>
<tr>
<th>Offsets from design position:</th>
<th>X = -4.4µm</th>
<th>X = +6.2µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y = +5.7µm</td>
<td>Angle = -0.01°</td>
<td>Y = -21.0µm</td>
</tr>
<tr>
<td>Angle = +0.13°</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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**Deca Technologies**

**Enabling a New Class: The Panel Level SoC**
Adaptive Patterning™ is key for cost & yield on large panel fan-out.

**Adaptive Routing***
Dynamically adapt RDL routing to accurately align to true die position

- BGA array fixed to package outline
- Enables multi-die fan-out

**Adaptive Alignment***
Align the entire RDL layer to true die position within the unit

- Enables high metal density designs
- Precise alignment of inductors to die

*Note: Patents issued & pending*
... advanced lithography capability for panel level SoCs

Planar surface with near term roadmap to 2µm line & space

Planarized interconnect surface
- Fine pitch capability
- Multi-layers of RDL
- Cu for low contact resistance

*Note: Patents issued & pending
... might panel based fan-out technology reshape our future?

with the possibility to...

Create panel level SoCs with optimized functional blocks
Slash SoC development time by an order of magnitude
Cut product development cost by factors
Enable system level SoCs for lower volume IoT applications
... industry pundits now believe fan-out is real

<table>
<thead>
<tr>
<th>Year</th>
<th>Billions of USD</th>
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<tbody>
<tr>
<td>2015</td>
<td>1</td>
</tr>
<tr>
<td>2016</td>
<td>2</td>
</tr>
<tr>
<td>2017</td>
<td>3</td>
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<tr>
<td>2018</td>
<td>4</td>
</tr>
<tr>
<td>2019</td>
<td>5</td>
</tr>
<tr>
<td>2020</td>
<td>6</td>
</tr>
<tr>
<td>2021</td>
<td>7</td>
</tr>
</tbody>
</table>

Source: TechSearch International, Yole Developpement & Deca Estimates

WLCSP = Fan-in Wafer Level Chip Scale Package
FOWLP = Fan Out Wafer Level Packaging

APU, Modem & most current WLCSP devices due to fan-out & protected fan-in

PMIC, CODEC, RFIC, other Analog

2015 Projection Fan Out Wafer Level Packaging Demand
Broad acceptance forecasted
… in summary

*We hold the power in our hands*
... in summary

We hold the power in our hands

... to transform electronic interconnect

... and create the panel level SoC of tomorrow
Thank You