Localized High Density Interconnects with Intel’s EMIB

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Acknowledgments

Background
Key Takeaways

- Increasing Demand for On-Package CPU-Memory Bandwidth & Capacity

- Dense MCPs are key Solution Path to enabling “Wide and Slow” High Bandwidth Busses

- The EMIB Dense MCP Architecture offers Localized High Density Interconnects to enable High BW links

1. High BW Links can also important for Heterogeneous Integration
HBM Is The High Bandwidth Solution

### Key Package Design Metrics
- Wires/mm of Die Edge
- Interconnects/mm²
- Signal Data Rate
- Energy/bit

### IO/mm/lyr
- FCXGA, FCCSP
- IO/mm/lyr = 28-34
- IO/mm/lyr 103*

*Oi et. al. 2014 ECTC report 2μm L/S, 25μm pad

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Source: www.skhynix.com
Abstract

In recent years there has considerable interest in packages that enable high wiring density between die. This interest is motivated by the need for high inter-die bandwidth using wide and slow data busses as a means of achieving low power (i.e. low pJ/bit) interconnects. This talk provides an introduction to Intel’s high wiring density packaging technology i.e. EMIB (Embedded Multi-Die Interconnect Bridge) and compares it with other alternative technologies.
Dense MCP Technologies
Performance Comparison Between on-Substrate and High Density on-Silicon Chip-to-Chip Wiring

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Typical on-Substrate Wiring</th>
<th>On-Silicon Wiring (Si Interposer or EMIB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wire Length</td>
<td>Up to 70mm</td>
<td>~0.5mm to 10mm</td>
</tr>
<tr>
<td>BW/lane</td>
<td>Up to 8.0GT/s</td>
<td>&gt;2.0GT/s</td>
</tr>
<tr>
<td>Power</td>
<td>1X pJ/b for &lt;10mm</td>
<td>1X pJ/b</td>
</tr>
<tr>
<td></td>
<td>1.3X pJ/b for &gt;10mm</td>
<td></td>
</tr>
<tr>
<td>IO Area</td>
<td>1X IO's / mm²</td>
<td>4X IO's / mm²</td>
</tr>
<tr>
<td>BW/mm</td>
<td>1X</td>
<td>5X</td>
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<tr>
<td>BW/mm²</td>
<td>1X GB/s / mm²</td>
<td>&gt;1X GB/s / mm²</td>
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On-Si Wires Will Provide Improved Bandwidth and Density

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However, silicon shows high insertion loss which can degrade performance of the whole system at the high frequency due to conductivity of substrate and additionally very high in cost resulting from the fine on chip metal processes. Also the size of silicon wafer and round shape limit the yield of interposer fabrication. Another possible substrate material is organic which has been used as a semiconductor packaging material for long time. Thus low cost and low loss organic can be used as an interposer substrate. However scaling of interposer substrate thickness and width/space of signal channels are limited for the organic interposer.
## Solutions* for High Density Die to Die Interconnects

<table>
<thead>
<tr>
<th>Benefits</th>
<th>Organic Substrate (2.1D)</th>
<th>Silicon Interposer (2.5D)</th>
<th>3D Die Stacking (3D)</th>
<th>EMIB</th>
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<td>• Standard assembly process</td>
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<td>• Utilizes existing substrate fabrication infrastructure</td>
<td>• CTE matched with active die.</td>
<td>• Short interconnect length for low power, and good signal integrity</td>
<td>• No limit to die sizes</td>
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<td>• Thin Cu layers blanket entire substrate.</td>
<td>• Interposer size is limited by reticle field and cost</td>
<td>• Process yields</td>
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<td>• Large micro-via pads limits multilayer routing density</td>
<td>• TSV capacitance can impact high speed signal integrity</td>
<td>• Thermal challenges</td>
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<td></td>
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<tr>
<td></td>
<td>• Higher Insertion Loss in Si</td>
<td>• Loss of design flexibility</td>
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<td></td>
<td></td>
<td></td>
<td>• Limited memory capacity</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td>• More complex organic substrate</td>
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* Non-TSV Interposers not included to keep things simple
# Si Interposer vs. EMIB

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• Standard assembly process | |

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| • Thin Cu layers blanket entire substrate.  
• Large micro-via pads limit multilayer routing density | • Interposer size is limited by reticle field and cost  
• Capacitance of TSV can impact high speed signal integrity | • Process yields  
• Thermal challenges  
• Loss of design flexibility  
• Limited memory capacity | • More complex organic substrate | |

Decision was made to compare the two best choices
Silicon Interposer Technology

Package Top View

Silicon Interposer

Die 1

Die 2

Die 3

Package Cross Section

Silicon Interposer

Conventional Organic Package

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Intel EMIB Technology

Embedded Bridge

Die 2

Die 3

Die 1

Embedded Bridge

Conventional Organic Package

Package Top View

Package Cross Section
EMIB Construction

An Alternative Architecture for High Density Multi-Chip Package Connections

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EMIB Bridge vs Silicon Interposer Fabrication

EMIB Fabrication is Simpler Than a 2.5D Interposer
EMIB vs Si Interposer Assembly

Typical 2.5D Interposer Process Flow

EMIB Process Flow

EMIB Assembly Eliminates a Chip Attach Module
EMIB vs. 2.5D Silicon Interposer: Evaluation Matrix

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<tr>
<th>Feature</th>
<th>Silicon Interposer</th>
<th>EMIB</th>
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<tr>
<td>Wiring Density</td>
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<tr>
<td>Chip-to-Chip Signal Integrity</td>
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<tr>
<td>Through Package Signal Integrity</td>
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<td></td>
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<tr>
<td>Through Package Power Delivery</td>
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<tr>
<td>Silicon Processing</td>
<td></td>
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<tr>
<td>Substrate Processing</td>
<td></td>
<td></td>
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<tr>
<td>Assembly Processing</td>
<td></td>
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<tr>
<td>Total Chip/Si Area on Package</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overall Cost</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Final Recommendation</td>
<td></td>
<td>✔</td>
</tr>
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</table>
Metal Layer Cross Section

EMIB

Silicon Interposer

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EMIB Mixed Bump Size & Pitch on Package

Variable Pitch Silicon Die Bumps

Cross-Section View of EMIB post-Assembly

Silicon Logic Die
Fine Pitch Bumps
Standard Pitch Bumps
Epoxy Underfill
What’s Next:
Can we take full advantage of new high density multi-chip package technology beyond HBM?
Heterogeneous Integration: Improve TTM, Functionality

- 2X Core Performance
- 5.5M Logic Elements
- Up to 70% Lower Power
- Up to 10 TFLOPS
- Most Comprehensive Security
- Intel 14 nm Tri-Gate
- Quad-Core Cortex-A53 ARM Processor

Heterogeneous System-in-Package (SiP) Integration
- Connectivity Tiles enable flexibility, scalability and fast time-to-market for new technologies

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Summary

• Demand for Densely Wired, High Bandwidth Multi-Chip Package Solutions is Very Strong

• Packages Require Silicon Backend Layer Wiring Densities to Satisfy Wiring Requirements

• Intel is Developing EMIB Packaging Technology as a Cost Effective, High Performance Solution for Localized High BW in Multi-Chip packages