Microelectronic Packaging Substrates: Future Challenges

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Agenda

• Overview of Microelectronic Packaging

• Flip Chip Substrate Scaling Challenges

• Intel’s New Packaging R&D Facility in Chandler

• Q & A
Roles of Semiconductor Packaging

- **Traditional Roles**
  - Space Transformation
  - Mechanical & Environmental Protection
  - Enhanced Thermal Solution
  - Platform for Component Identification

- **New expectations: provide solutions for**
  - high bandwidth signaling
  - more effective power management through embedded solutions
  - multifunction integration
  - form factor miniaturization

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First Level Interconnect (FLI)

Second Level Interconnect (SLI)
Silicon Scaling & Packaging Trends

Silicon Scaling requires Substrate Scaling, which calls for novel substrate materials and process technologies.
• Mass reflow (traditionally called C4) will be challenging for large dies with interconnect pitch < 100um interconnect & thin dies
Package Architecture Solutions

- Strong dependency on signal density and footprint
Agenda

• Si Scaling & Microelectronic Packaging

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Substrate Line Pitch Trend

Routing Line Pitch, μm

Source: ITRS

Key Challenges:

- Dry Film Adhesion at narrower trace space → Yield
- Trace Tolerance → Impedance Tolerance Control
- DE-to-Cu and Cu-to-DE adhesion → Reliability

Development of advanced, alternate technologies to achieve a low cost solution to enabling finer L/S (<10 μm) pitch
Future Alignment Requirements  

**Laminated Core Litho Alignment Demand**

**Build-up Litho Alignment Demand**

Mask-less Lithography (LDI) and lasers with tighter tolerance needed to enable future scaling

- <10/10um L/S
- Ultra thin packages
Metallization-Adhesion

Drivers
- Insertion loss
- Impedance variation
- FLS margin and yield
- Via integrity, MET/VET

Solutions
- Chemical adhesion promoter
- Seed layer sputtering
- Dry desmear
- Thin Cu transfer film

Extendable adhesion promotion technology required to meet electrical requirements and
Line Space < 5um.... Future Technology?

TCoO will decide the technology of choice!
Chandler CH8

- New R&D facility for advanced packaging
- $300M investment
- 285K square feet
- First tools docks July 1, 2013
Chandler 8

Intel Chandler CH-8
South East Elevation
December 2012 snapshot
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Q & A
Thank You!