Molded Interconnect System (MIS) Packaging Technology

Vinayak Pandey

May, 2016
MIS Substrate Introduction

**MIS**: Molded Interconnect System/Substrate

1LMIS substrate 4B 250x70mm (0.11mm thickness)

- **Carrier**
- **Pre-mold compound**
- **Surface finish** (Cu+OSP / NiAu / NiPdAu)
- **Finish plating**: NiPdAu, NiAu, Cu+OSP

**Routable**
- **Internal lead**
- **External lead**
- **Trace**
- **Pre-mold compound**
Drivers for MIS Package

• Drivers
  – Increase in I/O Density
  – Small, thin packages
  – Good electrical and thermal performance
  – Cost comparable to incumbent package or lower
  – Multiple packaging options

• Applications
  – Power Package (WB & fcQFN)
  – Mobile Processors (fcMIS)
  – Mobile chipsets (WB & FC MIS)
  – Applicable to leaded, laminate and SiP products
New solutions driving higher I/O density while managing total cost requirements
MIS provides a solution that can be used for leaded/laminate wirebond & flip chip packaging

QFN-dr/mr
FCQFN – FCOL/MIS
QFN
QFP

2L WB / 1L WB-SMS
(Single Metal Substrate)

1L WB - MIS

1/2L FC - MIS

2L FC - ETS

eWLB

FC – Flip chip
WB – Wirebond
SMS – Single Metal Substrate
ETS – Embedded Trace Substrate
MIS – Molded Interconnect Substrate
eWLB – Embedded Wafer Level Ball Grid Array
1L MIS Process Flow

Carrier

Mold compound

1L MIS

SPCC

1st plating

2nd plating

Dry film stripping

Molding

OR

ABF Lamination

Top side

Grinding

Window etch/Surface finish

Backside

<table>
<thead>
<tr>
<th>Item</th>
<th>MIS-a</th>
<th>MIS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trace/Stud Type</td>
<td>Cu</td>
<td>Cu</td>
</tr>
<tr>
<td>Filler Size(um)</td>
<td>2.2</td>
<td>45</td>
</tr>
<tr>
<td>Filler Content</td>
<td>82%</td>
<td>79%</td>
</tr>
<tr>
<td>CTE (ppm/K)</td>
<td>Alpha1=7</td>
<td>Alpha=11.1</td>
</tr>
<tr>
<td></td>
<td>Alpha2=21</td>
<td></td>
</tr>
<tr>
<td>Thermal Conductivity (W/mK)</td>
<td>0.65</td>
<td>1</td>
</tr>
<tr>
<td>Young's modulus(MPa)</td>
<td>7000</td>
<td>18500</td>
</tr>
<tr>
<td>Dielectric constant (DK), 5.8GHz</td>
<td>3.2</td>
<td>3.4</td>
</tr>
<tr>
<td>Td(deg-c)</td>
<td>DMA=167</td>
<td>TMA=172</td>
</tr>
</tbody>
</table>

ABF: Ajinomoto Build-up Film
MIS Substrate Introduction

Features & Advantage:

- Compatible for Au/ Cu/ Ag alloy Wire-Bonding and Flip Chip package
- Pin to Pin compatible with QFN, LGA and BGA Package
- Customized Design for Comprehensive Package
- Superior RF, Electrical, Heat and Reliability Performance
- Capable of Ultra Thin and Small Package (Package thickness: 0.31mm)
- Finer-Pitch Routable capability (L/S: Min.25/25um)
- No Die Shrinkage Constraint for Chip On Lead (COL)
- Compatible Multiple Chips/ paddles Module Packaging Application
- 3D-MIS Package Application (FC & Passive components)
- Capable of Built-in Inductors

MIS package with wire-bond process

MIS package with FC process
MIS Substrate Introduction

- 1L MIS package mass production from 2011,
  2L fcMIS package passed internal qualification, HVM in 2016
- Over 25 overseas customers
- Over 70 qualified packages mass production
- Flip chip & wire-bonding QFN-MIS production
- 95% volume Power & RF application.
- MSL 1 achievement

Wire-Bonding Chip On Lead (COL)
Flip Chip packaging
Extended Ground Pad
3D-MIS packaging (Die embedded)
Multi-Chips Module
Dual rows QFN Application
Multi-layer MIS Development

✓ Structure: FC-FBGA

✓ Technology comparison

Higher Cost

MSAP
Coreless
ETS
SAP
MIS
Tenting

50/50 40/40 35/35 30/30 25/25 20/20 15/15 10/10um
Multi-layer MIS Development

Process Flow of 2L MIS-a

1L Pattern Plating

Laminate Film Mold

Grinding

Electroless Plating

2L Pattern Plating

Laminate 2\textsuperscript{nd} Film Mold

Grinding

Window Stripping/ Surface Finish
Multi-layer MIS Development

Mobile Processor

Readout point Leg #1

TC’B’ 1000x w/ MSL3
O/S test Passed (77 / 77 units)

TC’B’ 1000x w/ MSL2aa
O/S test Passed (77 / 77 units)

✓ Reliability Results:

Qualified and HVM in 2016
Multi-layer MIS Development

2L MSAP Substrate

2L MIS Substrate (Film Mold + Cu)
Multi-layer MIS Development

2L MIS-a Packaging Construction Analysis

Flip chip on 2LMIS-a package

Microscope X-section view

Flip chip on Substrate
25um width trace

Microscope FC X-section view

Fc on MIS 40um trace
Multi-layer MIS Development

✓ Package with 4L SAP substrate

✓ Package with 3L MIS substrate

Advantages:
• Single material
• Thinner
• Low Warpage
• Achieve MSL 3
3D MIS Packaging

Characteristics:
- Passive Components
- Multi-chip Module
- 3D-MIS Substrate
- Large Area Metal and Partial Finer Line/Space

Advantages:
- Superior electrical and thermal performance
- Micro PMP
- High reliability performance
MIS Product Focus

• Routable QFN
  – Wire-bonding & Flip chip capable
  – Robust COL application
  – Sidewall wettable design for Automotive product (developing)
  – high I/O Dual Row QFN package
• Ultra-thin package - 0.31mm QFN/DFN package thickness
• 3D MIS Package
  – QFN-3D MIS Package
  – Package on Package (PoP) (developing)
  – RDL on Package (developing)
• Flip Chip CSP using single and multi layer MIS
• Higher reliability performance (MSL1) achievement
Thank You