Market Drivers for Advanced Packaging: 2020 and Beyond

E. Jan Vardaman, President and Founder

- TRACK INNOVATION
- IDENTIFY TRENDS
- ANALYZE GROWTH
- INFLUENCE DECISIONS

RELEVANT, ACCURATE, TIMELY

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Industry Trends

- **Trade friction continues to impact electronics industry**
- **Growth drivers for 2020**
  - PC sales are still slow (CPU shortage impacted 2019)
  - Smartphones shipment will see slight increase, driven by 5G
  - Server market expect to see an increase
  - Shift in interconnect from WB to FC for DRAM continues, especially in server market
  - IoT will see continue growth, especially for industrial
- **AI (including Edge) and HPC drives high-performance packaging**
  - Driving Si interposer, FO on substrate, high-density organic
  - Drives HBM (need more capacity)
  - High $ value, but low unit volumes
- **Automotive electronics**
  - Lower vehicles sales, but increased electronics content
Global Smartphone Shipments

- **Smartphone shipments expected to return to growth in 2020**
  - IDC projects a 1.5% growth in 2020 driven by China sales (2019 estimate to be 1.4B units)
  - IDC expects 190 million 5G smartphones to ship in 2020 (14% of total market)
  - Others have higher projections as much as 200 to 300 million units
  - Much of this is sub-6GHz

- **Billions of packages will be required**
  - More and larger packages in 5G phones
  - Good news for OSATs
• 5G New Radio required to handle high bandwidth, low latency and massive scalability of 5G
• 5G potentially means new radios, new modems, new PA, and new FEM
Examples of 5G Phones in Mass Production

- **Motorola 5G Moto Mod** for Z3/Z4
- **Samsung Galaxy S10 5G**
- **Oppo Reno 5G**
- **LG V50 ThinQ 5G**
- **Xiaomi Mi Mix 3 5G**
- **ZTE Axon 10 Pro 5G**
- **Huawei Mate 20X 5G**
- **OnePlus 7 Pro 5G**

Source: TechSearch International, Inc., adapted from TPSS.

RF/BB Packages and WLPs in Galaxy S10 5G

- Compared to S10, the S10 5G has 1.8x more of RF/BB packages with total package area that is 49% greater
- More WLPs
  - One WLP is a fan-in design run on the ASE/Deca M-Series FO-WLP production line

<table>
<thead>
<tr>
<th></th>
<th>S10 5G</th>
<th>S10/S10+</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total WLP Count</td>
<td>41</td>
<td>33</td>
</tr>
</tbody>
</table>

S10 5G package area 569 mm²
S10 package area 383 mm²
Global Rollout of 5G Services

- Telecoms in 18 countries will rollout 5G networks by the end of 2019
  - Speed of rollout depends on Telecom spending plan
- South Korea is global leader in 5G penetration (sub-6 GHz & mmWave)
  - 5G Subscriber base growth rate > 4G
  - Critical mass by end of 2020
- China’s 5G rollout main segment is sub-6 GHz (evolution of 4G)
- North America focused on sub-6 GHz & mmWave
- Europe focused on sub-6 GHz & mmWave
- Australia/SEA sub-6 GHz & mmWave

Source: GSMA, 2019
What Changes with 5G?

- 5G New Radio required to handle high bandwidth, low latency and massive scalability of 5G
  - Greater modularization, SiP designs with fully integrated antenna (so antenna design capabilities are important)
  - High-performance baseband processors
  - Broadband, steerable and high gain mmWave antennas
  - Efficient and broadband mmWave front-end ICs
  - RF components for co-design of mmWave antennas and front-end ICs with high-Q inductors, filters, power dividers, phase shifters, and attenuators

- New modems, new PAs, and new FEM, different filters for higher frequency
- Thermal and electrical modeling become more critical
- Electromagnetic compatibility and EMI shielding become more important
- New dielectric materials may be required for IC package substrate and PCB
- Test considerations
Sub-6 GHz vs. mmWave RF modules

- For sub-6 GHz RF modules, typically the antenna is on PCB
- mmWave RF modules antenna close to RF IC
- Both sub-6 GHz and mmWave modules require shielding

Source: Amkor Technology.
5G mmWave = Changes in Package Design and Construction

- 5G potentially means new radios, new modems, new PA, and new FEM
  - Greater modularization expected
  - System-in-package designs with fully integrated antenna (so antenna design capabilities are important)
  - Thermal and electrical modeling become more critical
  - Electromagnetic compatibility and EMI shielding become more important

- Antenna for sub-6 GHz can be on PCB, but mmWave needs RF IC closer to antenna, therefore antenna-in-package (AiP) design critical

Source: ASE.
5G FEM in Moto Mod

- The 5G Moto Mod attachment for the Motorola Z3 or Z4 handset has 5G front-end circuits and antennas for both sub-6 GHz networks and mmWave networks.

- Antenna arrays for mmWave connectivity are provided through four of Qualcomm’s QTM052 antenna-in-package modules:
  - Module is 19.15 mm x 4.83 mm x 1.74 mm
  - Contains RF transceiver (FC), PMIC (WLP), and passives
  - Array of phased mmWave antennas on underside

Source: TPSS.
5G Mobile RF Front-End AiP Module (28/39 GHz)

- Larger size SiP, more complex
- RF-FEM qualified by JCET in a 7mm x 19mm package
- EMI shielding required
- ABF build-up material requires flatter Cu surface (lower roughness) to minimize transmission loss
- Need balance between low insertion loss (Cu flatness w/ low Dk/Df substrate) and delamination (min. Cu roughness)

Source: JCET.

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Filter Requirements for 5G

- Acoustic wave filters (SAW and BAW) will not be suitable for millimeter wave (mmWave) version of 5G technology
- Different type of filters, such as waveguide or cavity, will be required
- New players offer filters are emerging, including start-up companies

Source: Taiyo Yuden.
5G and Infrastructure

- 5G promises higher data rates, lower latency, greater reliability, and larger capacity

- 5G infrastructure is moving into place with continued growth in 2020
  - Each macro base station will have a baseband unit, radio processing unit, and antenna typically packages in SiP
  - Four to five times as many micro base stations as macro base stations are projected

Source: IBM Assembly and Test (Bromont).
Comparison of PCB Material Factors by 5G Frequency Domain

- **Sub-6 GHz** same packaging methodology as 4G, similar SiP package design and existing supply chain (BOM)
- **mmWave** needs new package design for AiP with focus on substrate and EMI shielding

<table>
<thead>
<tr>
<th>Property</th>
<th>Sub 6 GHz</th>
<th>Millimeter-Wave (28 GHz to 39 GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate Thickness</td>
<td>Thicker (Typical 20 mils to 30 mils)</td>
<td>Thinner (Typical 5 mils to 10 mils) Thinned to avoid: unwanted resonances spurious modes excessive radiation</td>
</tr>
<tr>
<td>Dielectric Constant (Dk)</td>
<td>~3 to 3.7</td>
<td>~3 to 3.7 Lower values beneficial to enable wider traces at same characteristic impedance</td>
</tr>
<tr>
<td>Dissipation Factor (Df)</td>
<td>&lt;0.004</td>
<td>&lt;0.002</td>
</tr>
<tr>
<td>Copper Surface Roughness</td>
<td>Moderately significant</td>
<td>Very significant</td>
</tr>
<tr>
<td>Thermal Conductivity</td>
<td>&gt;0.5 W/(m-K)</td>
<td>&gt;0.5 W/(m-K)</td>
</tr>
<tr>
<td>Insertion Loss (Substrate thickness dependent)</td>
<td>Greater insertion loss</td>
<td>Lower insertion loss</td>
</tr>
<tr>
<td>Dominant Factor</td>
<td>Dielectric loss mostly related to Df</td>
<td>Conductor loss often due to surface roughness</td>
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5G mmWave Test Strategies in Mass Production

- 5G mmWave changing traditional cell phone architecture and test needs
- Use of antenna arrays require higher port count at mmWave frequencies
- Signal beam forming requires new and innovative test techniques

Source: Teradyne.
Servers for Datacenters

- Demand for datacenters from Alibaba Group Holding (China), Amazon, Apple, Google, Microsoft, Facebook, and Tencent Holdings (China) to run retail operations, search engines, cloud services, and social networks over the Internet
  - Demand slowed in 2019, but expected to pick up in 2020
- Demand for high-performance chips for data crunching drives demand for advanced packaging (flip chip packages)
  - New server packaging options including chiplets
- Demand for AI accelerators
  - Drivers demand for Si interposers and FO on substrate
- Demand for data storage driving growth in Flash memory (SSD)
- Demand for DRAM in DIMMs
Many Options for High Performance Packages

- **Silicon Interposers (in production today)**
  - Many examples of AI accelerators from Xilinx, NVIDIA (GPU + HBM), Google, Baidu, Huawei
- **Intel’s EMIB (in production today)**
  - Silicon bridge in an laminate substrate, embedded by substrate supplier
  - Intel Stratix 10 (FPGA + HBM2 on EMIB)
- **Fan Out on Substrate (in production since 2016)**
  - Many companies plan adoption for AI Edge applications
- **Organic Interposers (in development)**
  - Extend to finer feature (2μm L/S) switch to fab-like process
Cross-section of NVIDIA’s AI Package

- NVIDIA’s GPU with Cu pillar mounted on a 100µm-thick silicon interposer with TSVs using TSMC’s CoWoS process
- Four HBM with 8 DRAMs per stack plus logic layer are also mounted on the silicon interposer (HBM with 55µm pitch)
- Silicon interposer is 34 mm x 43 mm with 1.1µm lines and 1.6µm space
- Packaged on a 55mmx 55mm laminate substrate with 130µm pitch C4 bumps
**Intel Spring Crest (NNP-T) Neural Network Processor**

- **Nervana™ Neural Network Processor for Training**
  - Train complex deep learning models
  - Logic on TSMC CLN 16FF+ process
  - TSMC’s CoWoS technology
  - Nervana die size is 680 mm²
  - 1,200 mm² interposer
  - 32 GB HBM2

*Source: WikiChip Fuse*
Huawei Ascend 910

- Eight dies, total area 1,228 mm²
  - SoC 456 mm² + I/O 168 mm² + HBM 4 x 96 mm² + dummies 2 x 110 mm²
  - Dummy dies included for mechanical
  - SoC fabbed in TSMC 7+ EUV process
  - Record performance claimed

Source: Huawei
TSMC CoWoS

- **Largest silicon interposer from TSMC in production is 2,500 mm²**
  - >2X reticle size
- **Room for two, 600mm² processors + 8 HBM s in 75mm x 75mm package**

Source: TSMC.
EMIB Uses Si Bridge for Chip-to-Chip Communication

- Embedded Multi-die Interconnect Bridge (EMIB) A small silicon bridge chip is embedded into the package (no TSVs)
  - Substrate supplier embeds Si bridge
- EMIB allows the die I/O or bumps to be placed as close as possible to the edge of the die because fewer I/O or bumps are required
  - Micro bumps on chips, communication between chips through interposer
  - Provides a 2.5D localized high-density interconnect between the FPGA and the transceiver die

Source: TechInsights.
What’s Next?

- Intel’s Foveros
  - Active interposer
- TSMC’s SoI-C and WoW
  - System on Integrated Chip (SoI-C) 3D stack using CoW process to handle <10μm bond pitch between chips
  - Active interposer for SoI-C
  - WoW connects wafers with same size die
- New forms of 3D stacking (die-to-die interconnects) are coming
  - Die-to-wafer
  - Wafer-to-wafer attach
  - Hybrid bonding
- Co-design and thermal management essential

Source: TSMC.

Source: Intel.
Chiplets: Key Enabler for Next 10-20 Years

- **Chiplet demand driven by:**
  - Need for a more cost-effective solution given the economic challenging of continued silicon scaling
  - Desire to reuse IP
  - New test flows
  - Improved electrical performance
  - Reduced power consumption
  - Faster time-to-market

AMD’s Chiplet design on organic substrate

TSMC’s SoIC


Source: TSMC.
Intel Lakefield Hybrid CPU

- 10nm CPU, on 22nm active interposer
  - 12 x 12 x 1 mm package
- Standby power of ~2 mW
- Microsoft Surface Neo for 2020 holiday season
Package Choice in New Area Needs Careful Understanding

- Product life and reliability requirements
- Package design options (coupled with silicon strategy)
  - Design with system architecture point-of-view
- Thermal requirements
- Test needs
- Material interaction, impacted by
  - Thermal considerations
  - Supply chain
  - Cost (especially with respect to reliability)
Vehicle Sales Growth Trends

WW Automotive Sales (Million Units)

- Automotive sales slowed, but are expected to increase in future
- Electric vehicles account for a small percentage of sales
  - Drives growth in power devices

Source: IDC.
Advanced Driver Assistance Systems

ADAS System Forecast

- Increased use of safety features on the road to autonomous driving
- ADAS includes cameras, radar, ultrasonic, and LiDAR

Source: IDC
- Systems require image sensors and processing, OIS, power supplies, motor drivers, LED drivers, connectivity, ASICs, standard products, EEPROM

- Up to 10 cameras per luxury vehicle in 2020

Source: ON Semiconductor.
Tesla’s Autopilot 2.5 Board

- nVidia Parker SoC (nVidia Denver 2 + ARM Cortex A57 + Pascal GPU)
- SK Hynix GDDR5 DRAM
- Toshiba NAND Flash
- nVidia Pascal GPU (Discrete GPUs)
- Marvell Ethernet Switch (88EA6321-TFJ2)
- u-blox ADR Module with integrated 3D sensors (NEO-M8L series)
- Infineon MCU (TriCore AURIX)
Tesla: Switched to Internal Processor Design

- Telsa’s new internally designed processor (Samsung Austin fab)
- FC-BGA package
Packaging Issues: Substrate, Underfill, and TIM Materials

- Trace cracking seen for FC-BGA packages when qualified for automotive applications
- Underfill cracking driven by
  - Package design induced stress
  - Type of underfill material used
  - Process induced defects such as voids
  - Risk of cracking is higher with extended TC requirements for automotive
- Underfill process considerations
  - Must optimize the bump pitch scaling between process and reliability
  - Underfill flow time must be optimized to prevent voiding
  - Fine filler and/or lower filler loading may be required, but must be balance against thermo-mechanical requirements of CTE, fracture toughness, etc. that drive higher filler loading
  - New underfill materials and processes may be required
- Improved substrate performance is required to meet automotive reliability (no failures)
  - Package design optimization required
- New thermal interface materials may be required to handle high heat dissipation
Reliability Requirements for Automotive

- **Advances in automotive technology rely on new semiconductor and packaging technology**
  - Focus is on quality
  - Stakes are higher with ADAS and EV/HEV
  - No longer measure in parts per million (ppm) or parts per billion (ppb)
  - Measure in raw number of incidents
  - Only option is to screen or eliminate the defects (ZERO DEFECTS)

- **Audi**
  - 7,000 semiconductors per car
  - 4,000 cars produced per day
  - 1/ppm failure rate = 28 defective cars per day!

- **BMW**
  - 3,500 semiconductors per car
  - 10,000 cars per day
  - 1/ppm failure rate = 35 defective cars per day!
Expect the Unexpected!

- Passing AEC-Q-100, but can still fail at the next level
- **Problem:** Component passed AEC-Q 100 qualification
  - After board-level assembly, part failed qualification
  - Failure signature symptom showed interaction between component and board level has to be considered
  - Can’t just finish the qualification and leave everything else is up to the OEM or Tier-1
  - Typical automotive test requirements do not apply for autonomous driving!

**Mission Profile is an Input, not a check point**
**AEC is a check, not a real life test**
**Need standardized reference profiles!**
AI for Yield Enhancement: SVXR

- High resolution 3D X-Ray cross section
  - Pins flagged by machine learning
  - Verifies non-wet solder joints
- Al-based image processing
  - 100% inline process control and defect detection that improves over time
  - Many outliers detected by machine learning algorithm

**Unique SVXR Technology:**

100x Faster Imaging

SVXR’s Proprietary Detector:
30 mega-pixel, 65,000 gray-levels
Discussion from TechSearch International Workshops

- Reliability requirements have increased to 13 year application life and 150K kms travel distance (old specifications were 10 years and 100K miles)
- New standards are needed for BLR for future automotive applications as environmental use temperatures are increasing over current standards
  - Most of the existing standards are just test methods
  - Automotive suppliers are developing their own internal standards for each customer’s application
Conclusions

- **5G is coming**
  - Infrastructure roll out started
  - Modules with different package options, including AiP
- **Increased use of social media and IoT driving datacenter demand = high-performance packaging**
  - Growth for AI accelerators
  - AI accelerators demand drives use of silicon interposer and HBM
  - Si interposer proven technology, but alternatives emerging
  - Heterogeneous integration key to “economic limits of scaling”
- **Quest for autonomous driving**
  - Increased use of many types of sensors
  - AI solutions
  - Reliability key
Thank you!

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