Embedded SIP Modules For
Next-GEN Heterogeneous “Power-Devices”
with a section on non embedded Thick Cu Power Modules

Presented by
Nick Stukan Jr.
ACCESS Technologies USA
CMO & VP of Sales
Content

- Who is ACCESS Semiconductor
- Why Embedded Die PKG for Power Applications
- Roadmap, typical products & Reliability test Results
- Embedded Technology Outlook for 2019 and beyond
- Non Embedded Power applications (Thick Cu & Bar Vias)
Who’s ACCESS Semiconductor?

- China based focused to become a world wide provider of innovative High Density & Any Layer Interconnect (HD&ALI) IC Substrate & Embedded Die Package Technologies for the Semiconductor Industry.
- Established in 2006 in Zhuhai China, as a Via-post based “Coreless” organic IC substrate manufacturer.
- Advance device technology for embedded products includes; Thin IC’s, GaN, GaAs, and Monolithic “Power-Devices”:
  - HVM in 2 Layer “Single Die” Embedded μSiP Module
  - HVM in 4 Layer “Single Die Active + multi-Passives” Embedded SiP Module
  - In-Development on multi- “Actives + Passives” Embedded SiP Module
- ACCESS has 2 manufacturing sites in Zhuhai and Nantong, China.
ACCESS Fab A (Zhuhai)

ACCESS’s First Facility opened for Production in 2008
41,000 Sq. Meter Manufacturing floor
Equipped with via post, embedded die, tenting and mSAP technology
Serves the Mobile Handset, IOT, AI, HPC markets with RFPA, ASIC, FCCSP, Single Active Die Embedded and WB-BGA products
ACCESS Expansion **Fab B** (Nantong)

- ACCESS Nantong (under Construction) ready for Customer Qualification in Q4 2019
- Equipped with Via-Post, AmSAP, SAP & Advanced Embedded technologies. **Fab B is ready to serve the high-end Analog, Digital, HPC and Power Device markets.**
- Fab B is an Advanced facility with automation and smart manufacturing systems for HVM
- Fab B is 4 Times Larger than our Current Fab A at 160,000 Sq. Meters

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Value Proposition for Embedded Technology

- Size Miniaturization
- Design Effort Reduction
- Systematization
- High Efficiency
- Heat Dissipation
- Cost Reduction

Support on Advance Packages

- FOPLP & Embedded
- SiP
- FC-CSP/BGA
- Glass/Si Interposer

ACCESS Via-post Coreless Substrate Based

Power management

RFFE (PA/PAMiD, Switch, Filter, ASM)

Application Processor

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Next-Gen Power Devices ask for Embedded

WHY? System power is way too HIGH due to the need to drive long PCB traces between components which needs to be addressed quickly though advance device technologies such as; Silicon, GaN and GaAs are looking more promising every day!!!

ACCESS Embedded Solution Example:
A New Thermal Enhanced Embedded Structure

Embedded power modules show better heat dissipation than the conventional package over 20% improvements
Next-Gen Power Device ask for Embedded SiP

**WHY?** Next-generation SiP platforms are evolving rapidly to keep pace with emerging trends driven by an explosion of ‘POWER’ applications capabilities of delivering **higher performance, power efficiency and flexibility** simultaneously creating robust solutions.

ACCESS Embedded Solution Example:
A New *GaN* Embedded SiP Package

- High power density operation
- High switch frequency & Low loss
- High breakdown voltage
Embedded Die Development Trend Observed

- **Embedding of semiconductor chips into organic substrates** allows a very high degree of miniaturization by stacking multiple layers of embedded components, provides superior electrical performance by short and geometrically well controlled interconnects as well as a homogeneous mechanical environment of the chips, resulting in good Reliability and RoHS compliant.

- New manufacturing processes **combines mature PCB/substrate processing and die assembly in one production line** in order to benefit the most from this combination without the difficulties of transport between different manufacturing plants.
“Power” Requires Embedded as a SiP

- Power semiconductors has made **impressive progress increasing the power density** which is the primary **driving force behind power** system-in-package (SiP) and 3D power packages with heterogeneous functional integration.

- Heterogeneous SiP products are **Highly Integrated** semiconductors that **combines device technologies**; Si, GaAs, GaN with Passives, all within a **Single Embedded Package**.

- The Embedded SiP solution addresses all these **System level Challenges**:
  - Higher Bandwidth
  - Lower Power loss
  - Smaller foot-print or Form Factor
  - Increased Functional
  - Ability to Mix Process Nodes
  - To customize to meet the system requires.
  - “Lowest Cost of Ownership”
Technology Source For the ACCESS Embedded

ACCESS Semiconductor, is committed as a leader in the adaptation of **Embedding Die Package**, with over 13 years of mature **Coreless substrate** technology and proven track record for low profile dimensions with **seamless Ti/Cu sputtering** and Via-post/Cu Pillar interconnect giving advantages in **Electrical and Thermal** performance requirements at system level.
Embedded Process: “TPV-Frame”

- Organic Cavity Frame Prepare
- Die Pick&Place
- Laminate Dielectric ABF, Plasma etch
- Seed layer Sputter
- Patterning, Conductors Plating
- Solder Mask and Package Dice

Package with ACCESS!
Innovated Technical Advantages of ACCESS

- **Low Profile**: X/Y/Z Dimensions Reduce
  - No Need Wafer Bumping
  - Seamless Ti-Cu Sputtering
  - Copper pillar interconnection
  - Die face-up or Down

- **High Efficiency**: Fast Electro connection
  - High Power efficiency
  - High Heat dissipation

- **High Reliability**: Solid Frame To Prevent die Crack Above MSL3
  - Pass TC, HAST

- **Cost Effective**: Design
  - Material
  - Throughput

Focus on “Power Module”

- Standard Substrates/PCB Material
- No Need Wafer RDL process
- Skip high-k Over-Mold / Under-fill
- High utilization/throughput

5x5mm Pkg Example:
- 8” Wafer – 1K units
- 12” Wafer – 2.5K units

ACCESS Panel >10K units
New Supply Chain, New Business Model

Today, embedded chip process is being developed by printed circuit board (PCB) manufacturers creating a NEW supply chain, bringing NEW players into the semiconductor industry along with business models!
ACCESS Embedded Die Product Portfolio

- **Package with ACCESS!**

**Processor**

**Bio-sensor**

**Power**

**Fingerprint**

**RFFE**

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**Multi-layers**

- Single Die
  - GaN
  - 1 Face-down + 1 Face-up
  - GaN

- Multiple Dies
  - GaN
  - 1 Face-down + 2 Face-up
  - GaN or GaAs

- Die + Passives
  - Under development
  - Production
  - NPI

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What ACCESS can Provide

Single Die
- 1 Layer Fan-Out Package/Discrete
- 2 Layers Fan-Out SiP
- 2+2 Layers Double Sides Connection SiP
- 2+2 Layers Embedded chip SiP

Multiple Dies
- 2 chips Embedded Multi RDL Discrete
- 3 chips Embedded Multi RDL SiP
- chip + Components Embedded Multi RDL SiP

Die last
- Multi chip+passive, LVM 2019,Q4
- Multi chip Embedded Multi RDL SiP
- Multi chip/component Embedded Multi RDL SiP

Frameless

Embedded Product Examples
- Power
- Bio-sensor
- Enviro-sensor
- Fingerprint
- RFFE

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## Typical Embedded Structure Reliability Results

### 1) Single Die Embedded

<table>
<thead>
<tr>
<th>Rel. Test</th>
<th>Pre-condition</th>
<th>AC</th>
<th>HAST</th>
<th>TCC</th>
<th>TCG</th>
<th>HTSL</th>
<th>TCC100+AC48</th>
<th>EVB BI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Condition</td>
<td>MSL3, 260°C reflow *3</td>
<td>121°C/100%RH</td>
<td>130°C/85%RH,Bias</td>
<td>-65°C-150°C</td>
<td>-40°C-125°C</td>
<td>150°C</td>
<td>-65°C-150°C+121°C/100%RH</td>
<td>125°C, V&lt;sub&gt;max&lt;/sub&gt;</td>
</tr>
<tr>
<td>Duration</td>
<td>--</td>
<td>168hrs</td>
<td>96hrs</td>
<td>1000cys</td>
<td>2000cys</td>
<td>1000hrs</td>
<td>TCC96+AC48</td>
<td>1000hrs</td>
</tr>
<tr>
<td>Test Point</td>
<td>--</td>
<td>96/168h</td>
<td>--</td>
<td>240/500/750/1000</td>
<td>500/1000/1500/2000</td>
<td>500/1000h</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Test results</td>
<td>--</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
</tbody>
</table>
# Typical Embedded Structure Reliability Results

## 2) Single Die + Multi-layer

<table>
<thead>
<tr>
<th>Rel. Test</th>
<th>Pre-condition</th>
<th>AC</th>
<th>HAST</th>
<th>TCC</th>
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<td>150°C</td>
<td>-65°C-150°C+121°C/100% RH</td>
<td>125°C, Vmax</td>
</tr>
<tr>
<td>Duration</td>
<td>--</td>
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<td>96hrs</td>
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<td>2000cys</td>
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<td>--</td>
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<td>--</td>
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<td>500/1000/1500/2000</td>
<td>500/1000h</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Test results</td>
<td>--</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
</tbody>
</table>
# Typical Embedded Structure Reliability Results

## 3) Single Die multi layer + Passives

<table>
<thead>
<tr>
<th>Rel. Test</th>
<th>Pre-condition</th>
<th>AC</th>
<th>HAST</th>
<th>TCC</th>
<th>TCG</th>
<th>HTSL</th>
<th>TCC100+AC48</th>
<th>EVB BI</th>
</tr>
</thead>
<tbody>
<tr>
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<td>121°C/100%RH</td>
<td>130°C/85%RH, Bias</td>
<td>-65°C-150°C</td>
<td>-40°C-125°C</td>
<td>150°C</td>
<td>-65°C-150°C+121°C/100% RH</td>
<td>125°C, Vmax</td>
</tr>
<tr>
<td>Duration</td>
<td>--</td>
<td>168hrs</td>
<td>96hrs</td>
<td>1000cys</td>
<td>2000cys</td>
<td>1000hrs</td>
<td>TCC96+AC48</td>
<td>1000hrs</td>
</tr>
<tr>
<td>Test Point</td>
<td>--</td>
<td>96/168h</td>
<td>--</td>
<td>240/500/750/1000</td>
<td>500/1000/1500/2000</td>
<td>500/1000h</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Test results</td>
<td>--</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
</tr>
</tbody>
</table>

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Next Gen Platform: *Hybrid* Stack-up Solution

**ACCESS HVM Process**

POR: “TPV” frame + “Sputter+RDL” process

(Based on Via post “coreless”)

- ✓ Finer die pad pitch
- ✓ Shorter Cycle time
- ✓ Higher process capacity
- ✗ Lower power efficiency
- ✗ Lower thermal dissipation

**Hybrid Process** 2020Q2 ready

TPV” frame + PID on Die pad + MSAP

(Frame + PID + Laser drilling + Va filling plating + mSAP)

POR = Process of record; PID = Photoimageable dielectric material; MSAP = modified semi-additive process
Next Gen Platform: Die *First* or Die *Last*

ACCESS Embedded Technology is Actually Die First

ACCESS Coreless Cavity Substrate to Allow Die Last

**Why Die *Last***?
- High price chip solution
- High yield control
- Multi-Chip solution

ACCESS Via-post Advantage
Cavity: by etching through Copper pillars
ACCESS Embedded Key Differentiators

- Patented “Power Delivery” structure: using thick Cu Bar Vias, Any shape via
- Patented ‘Power Performance’ structure allows thin die with both sides exposed (embedded)
- Patented “Via-in-Frame” technology: to prevent die cracking (embedded)
- No Wafer Bumping: simplified supply chain, better time to market (embedded)
- Seamless Die to package interconnects for high current density: Sputtered seed layer, Stacked Vias
- Any Shape Via and High-Density Inductor capability
- SAP-like patterning process: Fine pitch L/S available (15/15um L&S & embedded trace)
- Hybrid dielectric capability (B-stage Prepreg & Film)
- Various Processes, Prepreg and Film Dielectrics Options: for performance, reliability and cost control

Strong IP & Know-how Protection Based on Years of Coreless HVM Experience.
ACCESS Outlook

- **FY2019**, will continue to be a niche *LVM high mix business*, more NPI Quals, Engineering Validations and Design Wins!

- **Target**, advance SiP Power Module with *multiple “Dies + Passives” platforms for next-Gen Si*, GaAs and GaN device technologies, with production ramp since 2018. ACCESS ships over 11 Million Embedded Active devices per month and increasing dramatically every quarter.

- **Develop**, *heavy 200um copper thickness for ACCESS RDL layer and Die Backside* to allow much higher power density

- **Hybrid**, with new *PID material for finer die pad pitch and additive process (MSAP/SAP) utilizing laser via technology* for cost-down capability by Q2FY2020.

- **Cost-Down**, *Strategy* focused on Embedded Technology COGS with *50% cost down* by 2025 through SiP Module optimization: Design, Technology, Equipment, Material and Process.

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<table>
<thead>
<tr>
<th>Structure</th>
<th>2018</th>
<th>2019</th>
<th>2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al/Cu pad pitch (μm)</td>
<td>155</td>
<td>125</td>
<td>125</td>
</tr>
<tr>
<td>Metal trace W / S (μm)</td>
<td>25/25</td>
<td>20/20</td>
<td>12/12</td>
</tr>
<tr>
<td>Dielectric thickness (μm)</td>
<td>25</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>Micro via size (μm)</td>
<td>60</td>
<td>60/50</td>
<td>60</td>
</tr>
<tr>
<td>Routing layer</td>
<td>2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Dielectric material</td>
<td>ABF GX-13 / GX T31/ LE-T15B/Photo-imageable material</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal finish</td>
<td>ENEPIG / NiAu / OSP</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**ACCESS Embedded Die Technology Roadmap**

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ACCESS Facilities

China, Nantong (Fab B)

China, Zhuhai (Fab A)

USA, California (RD/Sales Office)

HPC Computing

Coreless / PA Modules

Embedded Die
Application Examples
ACCESS Embedded Die Power Converter

Package Qual Yields: ACCESS 98.1% OSAT 99.74% Customer FT 98.45%

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Face Up/Down Dual die-in Package

After die placement

Face up and Face down dual Die in Package

Bottom View of two Dies in Package

Top View of two Dies in Package
ACCESS Embedded Die Heavy Heat Sink

Power Manager  5L Embedded Die Module

* 40µm Pillar+40µm thick Cu Plated Heat Sink

Package from diced, thin 12” wafer using ACCESS RDL
### ACCESS Embedded Die SiP RF Filter Package

**Unit size:** 5*3mm; **Die thickness** 100+/−15µm.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>ACCESS structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>SM</td>
<td>Solder Mask thickness (above metal)</td>
<td>15 ± 7µm</td>
</tr>
<tr>
<td>D1, D2, D3</td>
<td>Dielectric thickness</td>
<td>25 ± 7µm</td>
</tr>
<tr>
<td>D4</td>
<td>Dielectric thickness (Cavity frame)</td>
<td>130 ± 10µm</td>
</tr>
<tr>
<td>M1, M2, M3, M4, M5</td>
<td>Metal layers thickness</td>
<td>15 ± 5µm</td>
</tr>
<tr>
<td>TT</td>
<td>Total thickness</td>
<td>310 ± 40µm</td>
</tr>
</tbody>
</table>
ACCESS Embedded Die Power and Sensors

1.5L Embedded Die Module

Sensor

2L Embedded Die Module

Sensor

2L Embedded Die Module

Power Manager

4L Embedded Die Module

Power Convertor

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ACCESS Embedded Die **Emerging Applications**

- **LED Module**
- **2L Embedded Die Module**
  - ASIC
- **GaN Technology**
- **5L Embedded Die Module**
  - GaN Chip
- **Regulator**
- **3L Embedded Die Module**
  - Controller Chip

**GaN Technology**

Package with ACCESS!
Solution for High Power/Thermal

Non-Embedded HPC Applications

Heavy Copper Layer + Large Solid Bar-Shape Via

Form Factor  ↓  Temperature  ↓  Efficiency%  ↑  Package Rdson  ↓

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**Via Post Application:** Bar-shape Via (Thermal, high power)

### Via design item

<table>
<thead>
<tr>
<th>Bar-shape Via</th>
<th>Production Design Rule</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Dielectric thickness</td>
</tr>
<tr>
<td></td>
<td>30, 35 or 40</td>
</tr>
<tr>
<td>Width (Min/Max)</td>
<td>60/1000</td>
</tr>
<tr>
<td>Length (Min/Max)</td>
<td>60/1000</td>
</tr>
<tr>
<td>Space</td>
<td>80</td>
</tr>
<tr>
<td>Area%</td>
<td>≤35% of unit area</td>
</tr>
</tbody>
</table>

### Bar-via size tolerance

- Annular ring: ≥ 20

**Unit:** µm

**Top view**

**X-section**
High Copper Ratio Performance: Efficiency & Heat

Increasing Copper% of via array Under Chip

- Original (Laser drill array) 11%
- Bar-shape (Via post) 42%
- Plated Slug (Via post) 83%
- Cavity 100%

Working Temperature Simulation

- 123°C
- 110°C
- 100°C
- 94°C

Die

Die-1 Flip Chip

Die-2 Wirebond Chip

Bar via array under Flip Chip

Working Temperature Simulation

- 97
- 96
- 95
- 94
- 93
- 92
- 91
- 90
- 89
- 88
- 87
- 86
- 85

Eff (%)

I out (A)

ACCESS Other supplier

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Plated Heat Spreader

PHS can be up to 55% of unit area

<table>
<thead>
<tr>
<th>Top view</th>
<th>4 Layers</th>
<th>6 Layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Back view</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| Cross section view |

<table>
<thead>
<tr>
<th>Production Design Rule per Dielectric thickness (35/60/80/100/130µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Via design item</strong></td>
</tr>
<tr>
<td><strong>Bar-shape Via</strong></td>
</tr>
<tr>
<td><strong>Space (Min)</strong></td>
</tr>
<tr>
<td><strong>Bar-via size tolerance</strong></td>
</tr>
<tr>
<td><strong>Annular ring</strong></td>
</tr>
</tbody>
</table>

Unit: µm

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Thank You!

Package with ACCESS!

For more information or to schedule a meeting please contact Beth Perrelli at beth@access-substratesusa.com
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Cupertino, CA 95014

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